M88DR5CK01

Gen1 DDR5 Clock Drive (CKD)
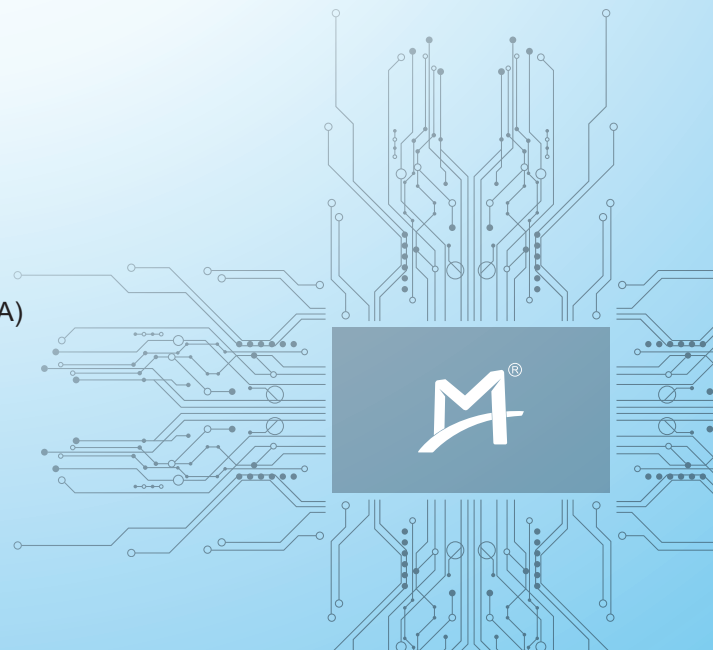
General Description

M88DR5CK01 is Montage's 1st-generation DDR5 Clock Driver (CKD) chip for use in the client memory to enhance the speed and stability of memory data access, matching the ever-increasing CPU operating speed and performance. The chip is compliant with the JEDEC DDR5CKD01 specification and supports data rates up to 7200MT/s. It supports double-sided bus address access and I²C, I3C interfaces. By configuring register control words, the chip can change its output signal characteristics to match the network topology of different DIMMs, and unused output signals can be disabled to reduce power consumption.
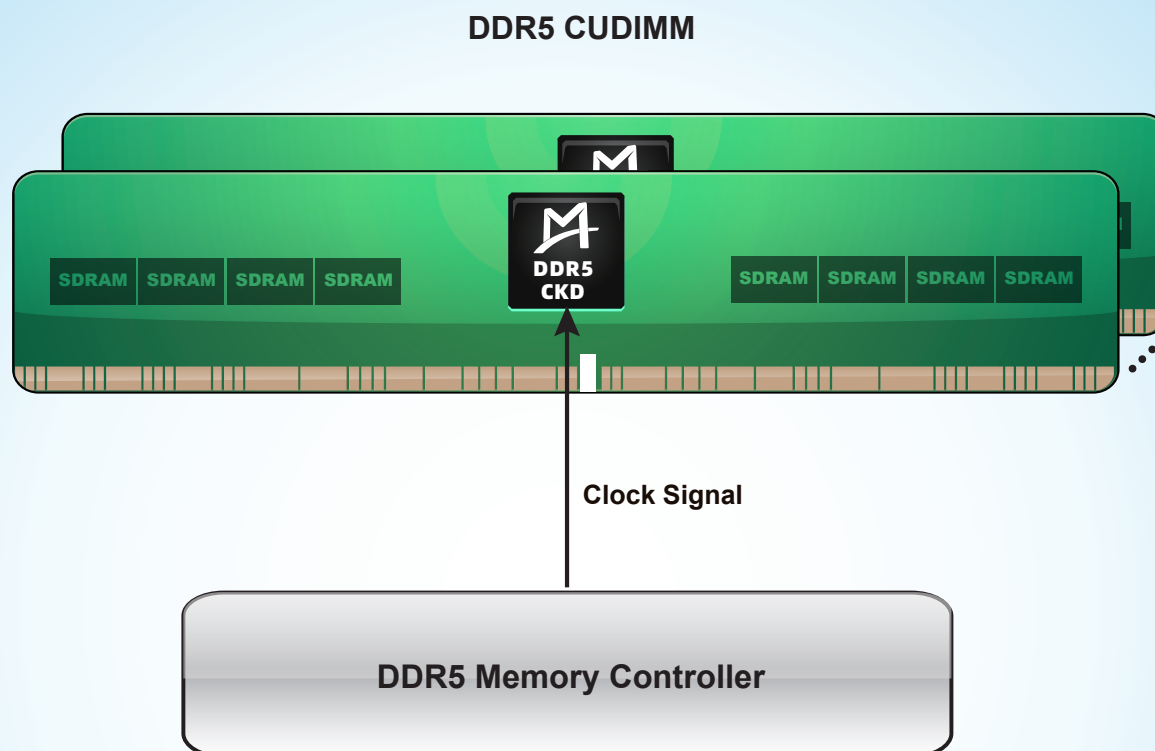
Applications

- DDR5 CUDIMM, CSODIMM and CAMM

Feature List

- Fully compliant with JEDEC Clock Driver Definition (DDR5CKD01) specification
- Support speed up to DDR5-7200
- 1.1V VDD voltage
- Output characteristics configurable through control registers
- Clock driver with zero phase delay
- Programmable latency per channel
- I²C and I3C Basic interface
- Dual sideband Bus address
- Ultra-low power consumption
- RoHS compliant
- Green package: 35-ball Fine-Pitch Ball Grid Array (FPBGA)

Application Diagram

DDR5 CUDIMM

| SDRAM | SDRAM | SDRAM | SDRAM | | DDR5 CKD | | SDRAM | SDRAM | SDRAM | SDRAM |

Clock Signal

DDR5 Memory Controller

Notes: Here shows the application of CKD on the DDR5 CUDIMM as an example.

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