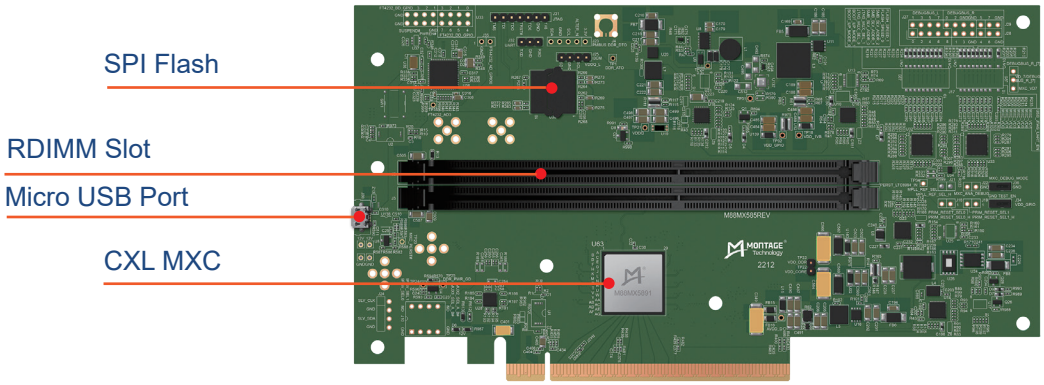
M88MX5891/5851

CXL® Memory eXpander Controller

Introduction

M88MX5891/5851 is a Compute Express Link® (CXL®) Type 3 Memory eXpander Controller (MXC) used to provide high-speed, low-latency interconnect between CPU and CXL-based devices. The MXC integrates a CXL controller, a DDR controller, a RISC-V micro-processor and rich peripheral interfaces such as SMBus and I3C/I²C in a single chip. It is compliant with JEDEC DDR4/DDR5 standards and CXL 2.0/PCIe® 5.0 specifications.

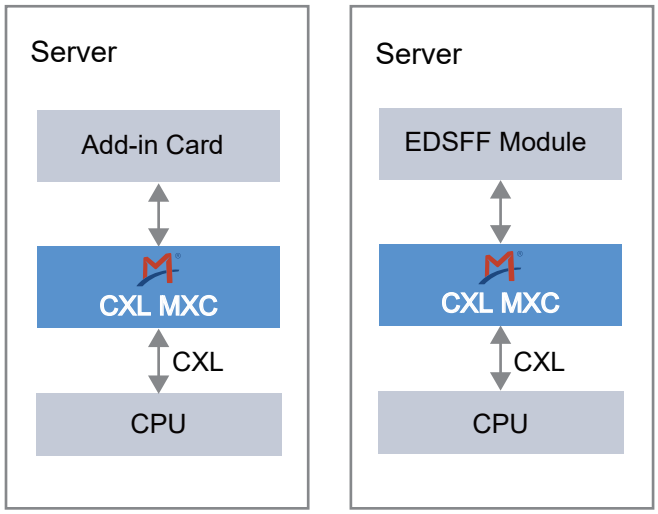
As the key component for memory expansion and pooling, the MXC is designed for use in add-in cards and EDSFF memory modules, which enables dramatically scaling of memory capacity and bandwidth to meet the ever-growing demand from HPC and AI applications.



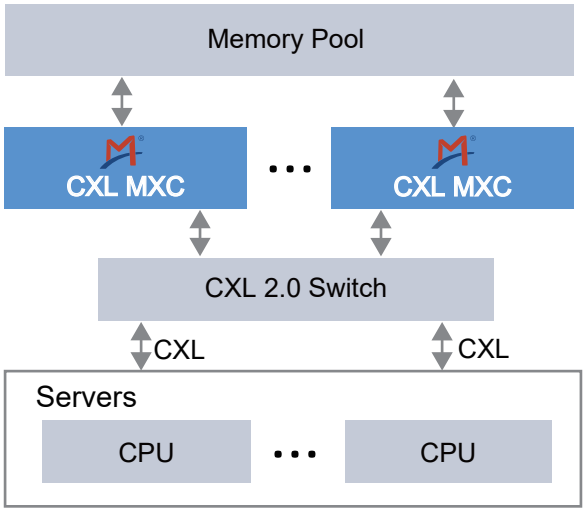
CXL MXC Evaluation Board (DDR5 RDIMM)

Typical Applications

- Add-in card or EDSFF memory module for memory expansion, memory pooling, etc.
- AI, machine learning, cloud infrastructure, high-performance computing, etc.



Memory Expansion



Memory Pooling

Features

CXL Type 3 Memory eXpander Controller

- Integrated CXL controller, DDR controller and RISC-V micro-processor
- On-chip PVT sensor
- SMBus, I3C/I²C, SPI interfaces
- Package: 767/716-ball FCCSP

CXL Controller

- Compliant with CXL 1.1 and CXL 2.0 RAS specifications, supporting CXL.mem and CXL.io protocols
- Designed based on PCIe 5.0 interface, supporting up to 32 GT/s (x8 lanes)
- Rich RAS features

DDR Controller

- Compliant with JEDEC DDR4/DDR5 standards
- Support DDR4/DDR5 UDIMM/RDIMM and DRAM on-board
- Low power consumption
- Optimized DDR I/O equalization and programmable I/O impedance

Software for Evaluation Board

Main Features:

- Flash Content Update
- Chip Configuration Change
- Mailbox Command
- Memory Error Injection
- CXL/DDR Eye Diagram Drawing