Description

M88MX6852 is a Compute Express Link® (CXL®) Type 3 Memory eXpander Controller (MXC) designed for memory expansion and memory pooling. It supports CXL.mem and CXL.io protocols and integrates a CXL controller based on the PCI Express® (PCIe®) infrastructure to leverage the PCIe 6.2 physical and electrical interfaces. While supporting speeds up to 64 GT/s with x8 lanes, it can also flexibly downgrade to lower speeds. The CXL link can also be bifurcated to dual x4 ports.

Compliant with the DDR5 specification, M88MX6852 supports DDR5 UDIMMs/RDIMMs and DDR5 DRAMs soldered on PCBs. Designed with two internal DDR5 memory controllers, M88MX6852 provides two independent DDR5 channels up to 8000 MT/s. The CXL memory requests are translated to DDR commands for data transactions between the CPU host and the DRAMs or DIMMs behind M88MX6852.

M88MX6852 has two built-in RISC-V micro-processors to manage all the subsystems inside the device, namely, the application process unit (APU) for applications such as DDR/CXL configuration and runtime event/interrupt service and the security process unit (SPU) for SoC security operations.

The device also supports SMBus/I3C interfaces on the host side for management purpose and I3C/I^2C interfaces at the media side for DDR5 applications. In addition, it supports SPI interfaces for external Flashes and JTAG and UART ports for debug purposes.

Features

DDR Subsystem

- Compliant with JEDEC DDR5 specification
  - DDR5 UDIMMs/RDIMMs and DDR5 DRAMs soldered on PCBs
  - x4 and x8 SDRAMs
  - DDR5 3DS (up to 8H)
  - 2 independent DDR channels
  - 1, 2 or 4 memory ranks per channel
- Speed up to DDR5-8000
- 1N and 2N modes supported
- 72-bit and 80-bit data path widths
- BL16 supported
- BL18 MRR supported
- Low power consumption
- Rich RAS features

CXL Subsystem

- CXL 1.1/2.0/3.1
- PCIe/CXL.io base
  - Single port with x8 lanes
  - Dual ports with x4 lanes
  - Data rate up to 64 GT/s
- CXL IDE
- CXL DVSEC
- Type-3 Single Logical Device (SLD)
- Type-3 MLD in single port mode (2 LDs)
- Dynamic Capacity Device
- Vendor Defined Message (VDM) for CXL power management
- CXL Memory Mapped IO (MMIO) registers
- Mailbox
- Data Object Exchange (DOE) instances
  - CDAT DOE
  - Compliance DOE
  - Security DOE
- Low latency mode
- Datapath protection for RAS
- CXL Performance Monitoring Unit (CPMU)

Overall System Features

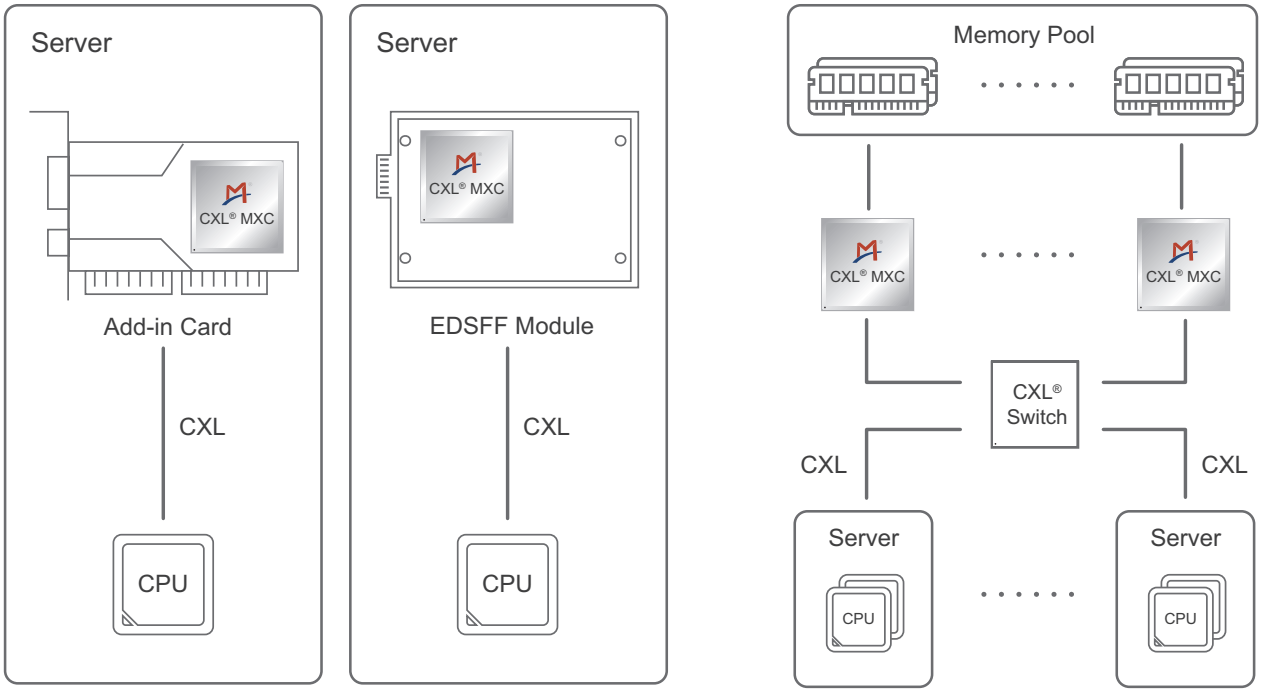
- Built-in RISC-V MCUs for security and application respectively
- On-chip PVT sensors
- Peripheral interfaces
  - SMBus/I3C/I^2C interface
  - SPI interface for external Flash
  - JTAG port
  - UART port
- Green package: 1211-ball FCBGA
- RoHS compliant

Applications

- AIC/EDSFF memory module for memory expansion and memory pooling
- Machine learning, cloud infrastructure, compute-intensive applications, next-generation computing, etc.

For more information on the product, please contact globalsales@montage-tech.com

Typical MXC Application Scenario



Memory Expansion **Memory Pooling**