Description

M88MX5851 is a Compute Express Link® (CXL®) Type 3 Memory eXpander Controller (MXC) designed for memory expansion and memory pooling. It supports CXL.mem and CXL.io protocols and integrates a CXL controller based on the PCI Express® (PCIe®) infrastructure to leverage the PCIe 5.0 physical and electrical interfaces. While supporting speeds up to 32 GT/s with x8 lanes, it can also flexibly downgrade to lower speeds.

Compliant with the DDR5 specification, M88MX5851 supports DDR5 UDIMMs/RDIMMs and DDR5 DRAMs soldered on PCBs. Designed with an internal DDR5 memory controller, M88MX5851 supports dual sub-channel DDR5 up to 6400 MT/s. The CXL memory requests are translated to DDR commands for data transactions between the CPU host and the DRAMs or DIMMs behind M88MX5851.

M88MX5851 has a built-in RISC-V micro-processor to manage all the subsystems inside the device. It is responsible for device initialization, configuration, error handling, and other features like temperature monitoring.

The device has an SMBus interface on the host side for management purpose and an I3C/I^2C interface at the media side for DDR5 applications. In addition, it supports SPI interfaces for external Flashes and JTAG and UART ports for debug purposes.

Features

DDR Subsystem

- Compliant with JEDEC DDR5 specification
  - DDR5 UDIMMs/RDIMMs and DDR5 DRAMs soldered on PCBs
  - x4 and x8 SDRAMs
  - DDR5 3DS (up to 8H)
  - 1, 2 or 4 memory ranks
- Speed up to DDR5-6400
- 1N and 2N modes supported
- 72-bit and 80-bit data path widths
- BL16 supported
- BL18 MRR supported
- Low power consumption
- Rich RAS features

CXL Subsystem

- CXL 1.1/2.0
- PCIe/CXL.io base
  - Single port with x8 lanes
  - Data rate up to 32 GT/s
- CXL IDE
- CXL DVSEC
- Type-3 Single Logical Device (SLD)
- Vendor Defined Message (VDM) for CXL power management
- CXL Memory Mapped IO (MMIO) registers
- Mailbox
- Data Object Exchange (DOE) instances
  - CDAT DOE
  - Compliance DOE
  - Security DOE
- Low latency mode
- Datapath protection for RAS
- CXL Performance Monitoring Unit (CPMU)

Overall System Features

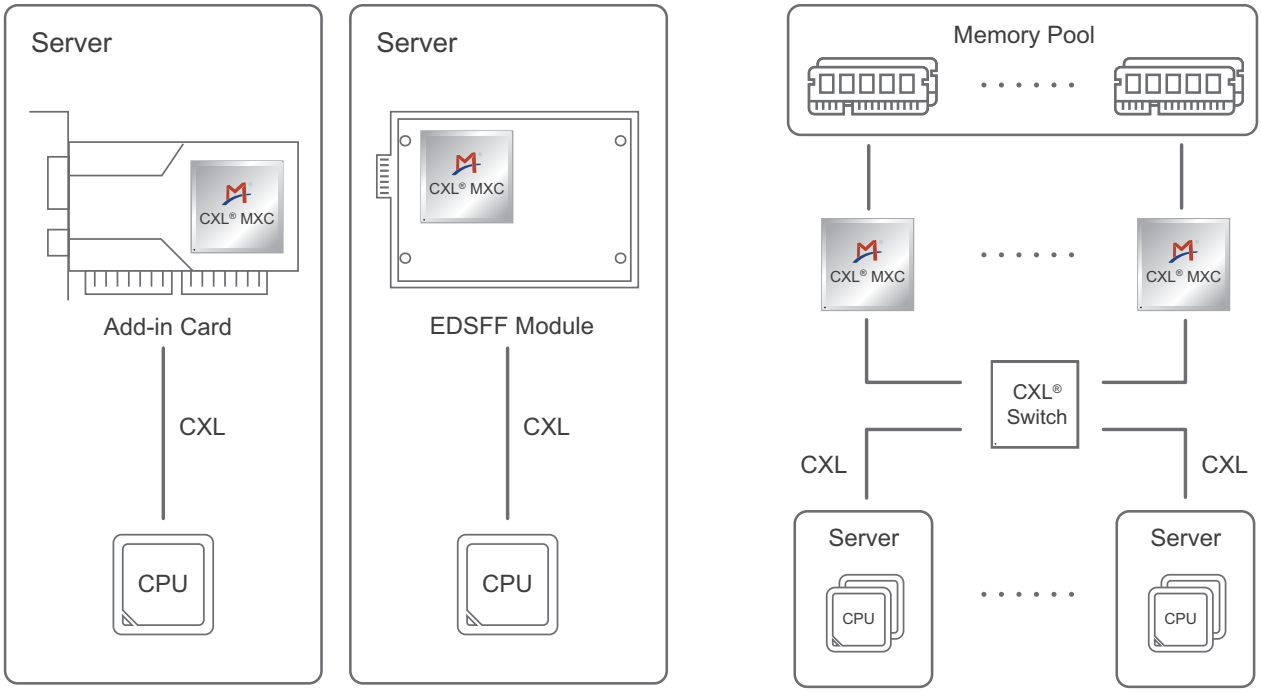
- Built-in RISC-V micro-processor
- On-chip PVT sensors
- Security features
- Peripheral interfaces
  - SMBus/I3C/I^2C interface
  - SPI interface for external Flash
  - JTAG port
  - UART port
- Green package: 716-ball FCCSP
- RoHS compliant

Applications

- AIC/EDSFF memory module for memory expansion and memory pooling
- Machine learning, cloud infrastructure, compute-intensive applications, next-generation computing, etc.

For more information on the product, please contact globalsales@montage-tech.com

Typical MXC Application Scenario



Memory Expansion **Memory Pooling**