Description

The M88TB(S)Qxxx[1,2,3] family consists of high-performance clock fanout buffers with 20, 16, 12, 8, or 4 LP-HCSL differential outputs, making them ideal for high-speed, low-jitter clock distribution in server platforms as well as networking, computing, and PCIe-based systems.

Selected buffers in this family are fully compatible to Intel® DB2000Q, DB2000QL, or DB1206 specifications. Operating from either a 3.3V or 1.8V power supply, the buffers deliver ultra-low additive phase jitter that meets PCIe Gen 7 reference clock requirements. The outputs support 85Ω or 100Ω impedance options to accommodate a wide range of system environments. The buffers offer flexible input clock configurations, including direct HCSL/LVDS connections and optional AC-coupled inputs with internal bias and termination control.

To enhance system reliability, the buffers integrate a reference loss detection circuit that continuously monitors the input clock pair. Output enable and configuration are supported through three control interfaces: SMBus, dedicated OE# pins, and SBI.

Features

General

- Ultra-low additive phase jitter:
  - PCIe® Gen 5: 4.3fs RMS
  - PCIe® Gen 6: 2.6fs RMS
  - PCIe® Gen 7: 2.2fs RMS
  - 12kHz to 20MHz additive phase jitter: 28fs RMS at 156.25MHz
- Latency & Skew
  - Consistent low latency from reference input to all outputs
  - Ultra-low output-to-output skew
  - Minimal part-to-part skew ensures reliable multi-device clock synchronization
- 3.3V or 1.8V power supplies
- Working temperature: −40°C to +105°C

1. TB: Buffer.
2. TBS: Two-input buffer with switchover.
3. Please refer to Ordering Information for the complete list of part numbers.

Input Clock

- One or two input reference clocks:
  - Supports DC and AC coupling
  - Supports frequencies from 1MHz to 400MHz

Output Clock

- 20/16/12/8/4 LP-HCSL differential output clocks
- 85Ω or 100Ω output impedance (100Ω for H-suffix buffers)

Control

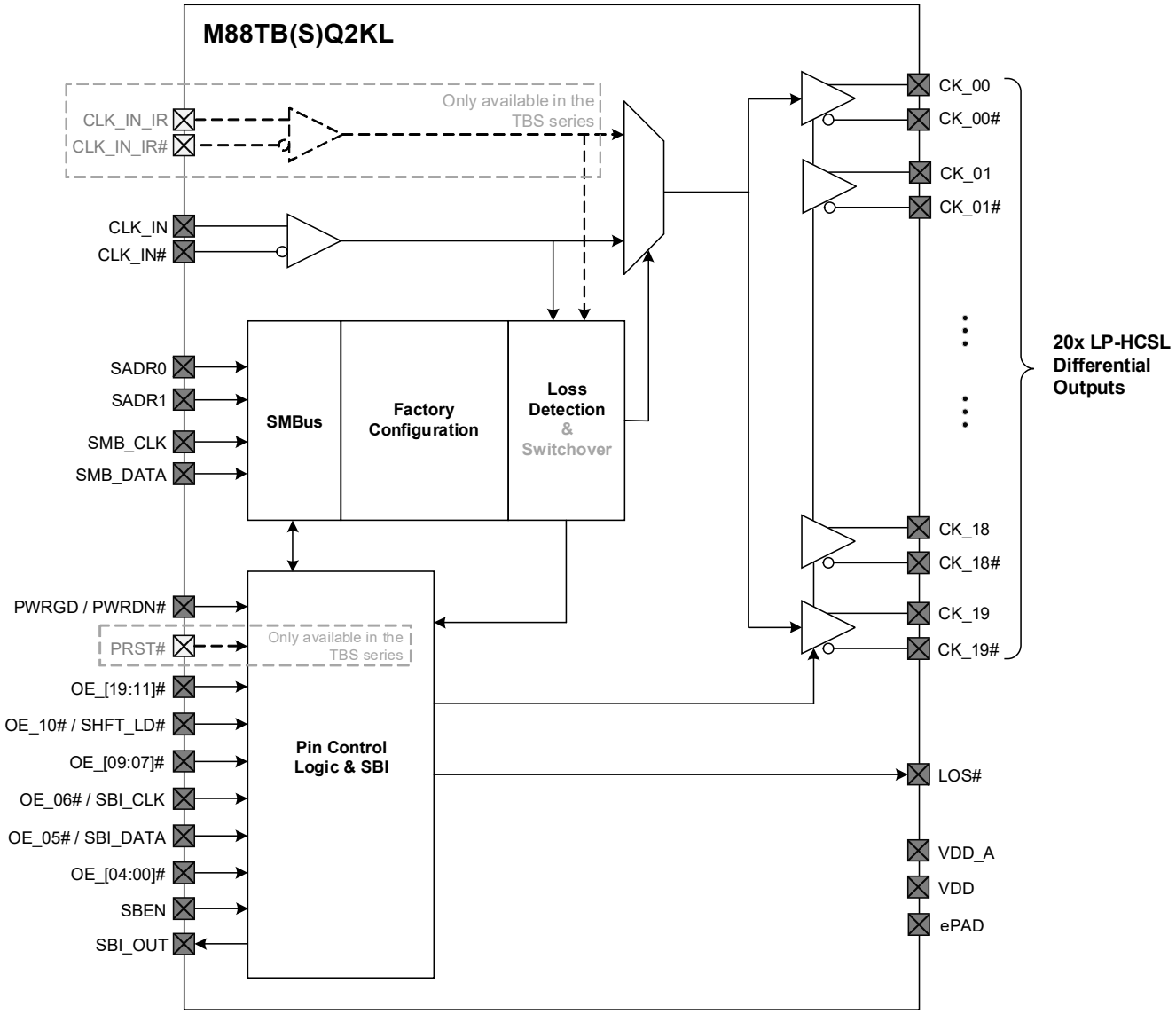
- SMBus interface with nine device addresses and I^2C-compatible
- Intel-compliant Side-Band Interface (SBI), supporting a daisy-chain topology
- Automatic output disable
- Glitch-free reference switchover (TBS series only)

Applications

- PCIe Gen 1 to Gen 7 and NVLink
- NVMe storage
- Cloud/Large-scale data analytics
- Networking

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Functional Block Diagram



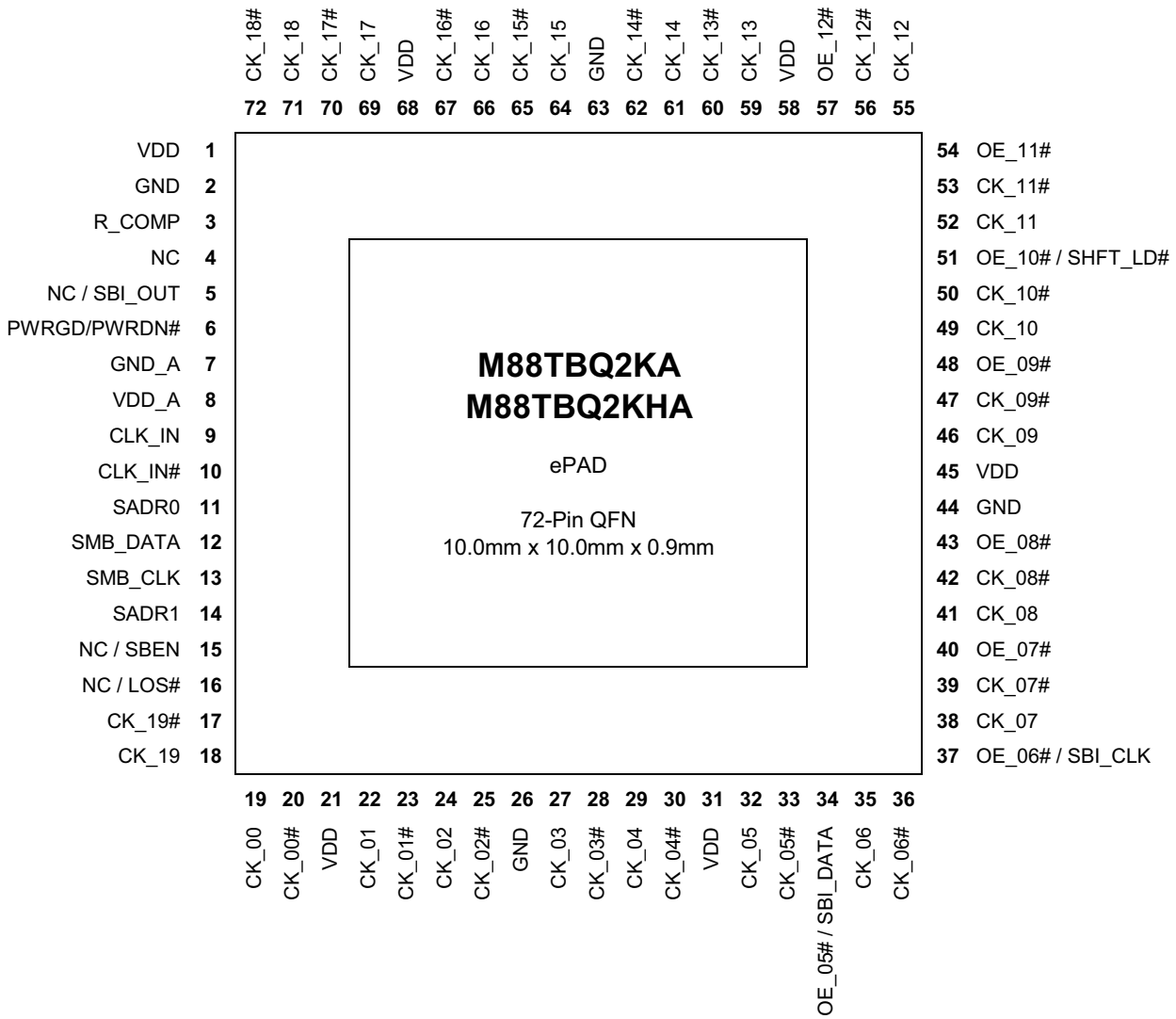
Notes:

1. Using M88TB(S)Q2KL as an example, this block diagram shows the full feature set of the clock buffers.
2. The availability of OE_n# and CK_n / CK_n# signals (where *n* = 00, 01, ..., 19), as well as pin multiplexing, varies depending on the specific part number.
3. Switchover function is supported in the TBS series only.
4. For a complete list of part numbers and their supported features, please refer to Ordering Information.

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Pin Assignment

Figure 1. M88TBQ2K Pin Assignment



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Figure 2. M88TBQ2KL Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	
A	CK_17	CK_16#	CK_16	CK_15#	CK_15	CK_14#	CK_14	CK_13#	CK_13	CK_12#	CK_12	CK_11#	A
B	CK_17#	VDD	NC/ OE_16#	SADR0	NC/ OE_15#	VDD	NC/ OE_14#	SADR1	NC/ OE_13#	OE_12#	VDD	CK_11	B
C	CK_18	NC/ SBI_OUT									OE_11#	CK_10#	C
D	CK_18#	NC/ OE_17#									NC/ OE_18#	CK_10	D
E	CK_19	SBEN									OE_10#/ SHFT_LD #	OE_09#	E
F	CK_19#	NC									NC	CK_09#	F
G	CLK_IN	NC									NC/ LOS#	CK_09	G
H	CLK_IN#	VDD_A									OE_08#	CK_08#	H
J	CK_00	NC/ OE_00#									NC/ OE_19#	CK_08	J
K	CK_00#	NC/ OE_01#									OE_07#	CK_07#	K
L	CK_01	VDD	NC/ OE_02#	SMB_DA TA	SMB_CL K	NC/ OE_03#	NC	OE_05#/ SBI_DAT A	NC/ OE_04#	OE_06#/ SBI_CLK	VDD	CK_07	L
M	CK_01#	CK_02	CK_02#	CK_03	CK_03#	PWRGD/ PWRDN#	CK_04	CK_04#	CK_05	CK_05#	CK_06	CK_06#	M
	1	2	3	4	5	6	7	8	9	10	11	12	

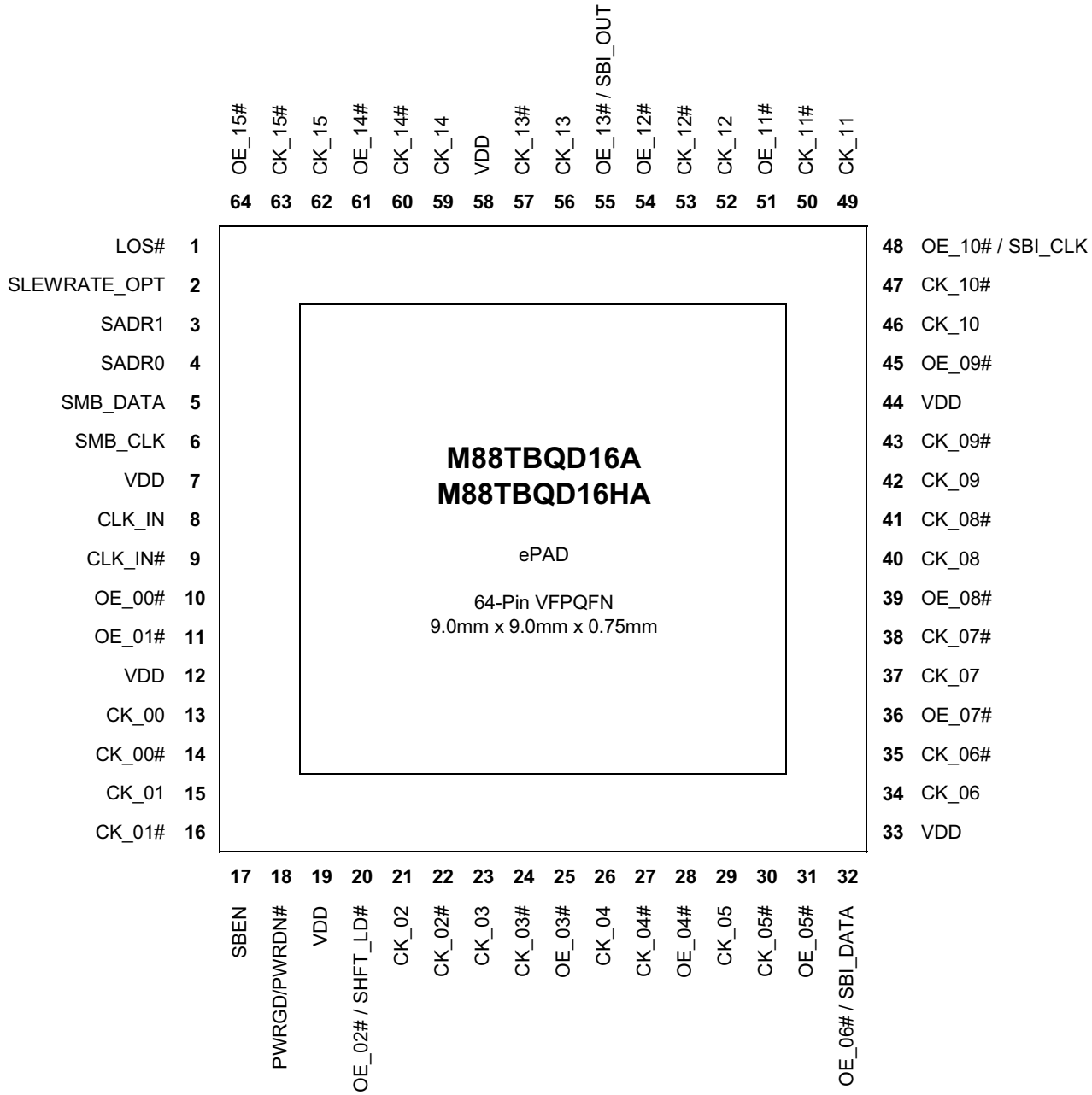
M88TBQ2KLA
M88TBQ2KLHA

ePAD

80-Pin GQFN
6.0mm x 6.0mm x 0.75mm

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Figure 3. M88TBQD16 Pin Assignment



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Figure 4. M88TBQD12 Pin Assignment

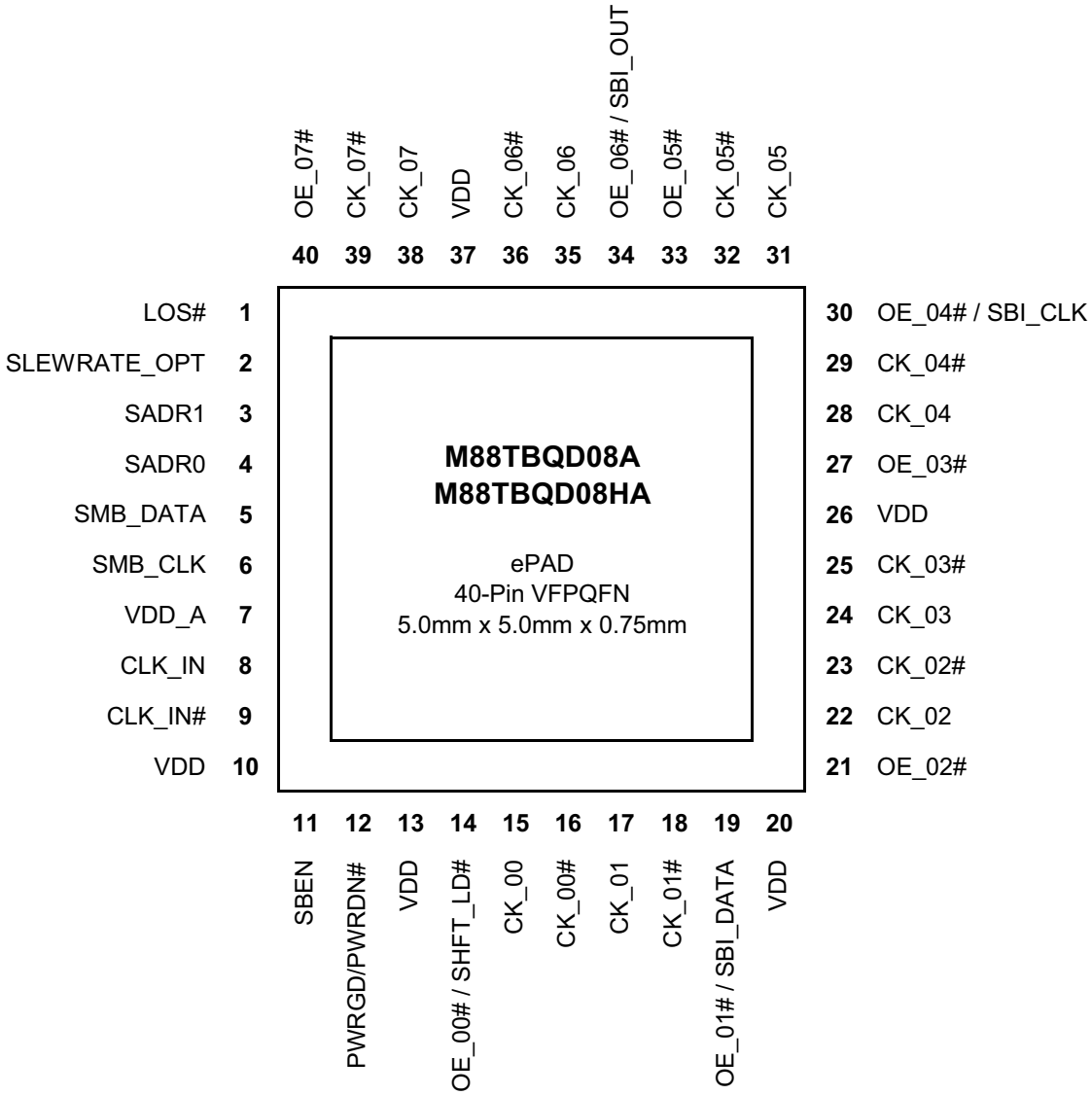
	1	2	3	4	5	6	7	8	9	10	
A	LOS#	CK_00#	CK_00	CK_01#	CK_01	CK_02#	CK_02	CK_03#	CK_03	OE_04# /SBI_CLK	A
B	SADR1	NC	OE_00#	OE_01#	VDD	NC	OE_02# /SBI_OUT	OE_03#	NC	CK_04#	B
C	SADR0	SLEWRATE _OPT							VDD	CK_04	C
D	SMB_CLK	SMB_DATA		GND	GND	GND	GND		NC	CK_05#	D
E	CLK_IN	NC		GND	GND	GND	GND		OE_05#	CK_05	E
F	CLK_IN#	VDD_A		GND	GND	GND	GND		NC	CK_06#	F
G	OE_11#	NC		GND	GND	GND	GND		OE_06#	CK_06	G
H	CK_11	VDD							VDD	CK_07#	H
J	CK_11#	NC	VDD	OE_10#/ SHFT_LD#	NC	OE_09#	NC	OE_08#	NC	CK_07	J
K	SBEN	PWRGD/ PWRDN#	NC	CK_10	CK_10#	CK_09	CK_09#	CK_08	CK_08#	OE_07#/ SBI_DATA	K
	1	2	3	4	5	6	7	8	9	10	

M88TBQD12A
M88TBQD12HA

64-Pin LGA
5.0mm x 5.0mm x 0.66mm

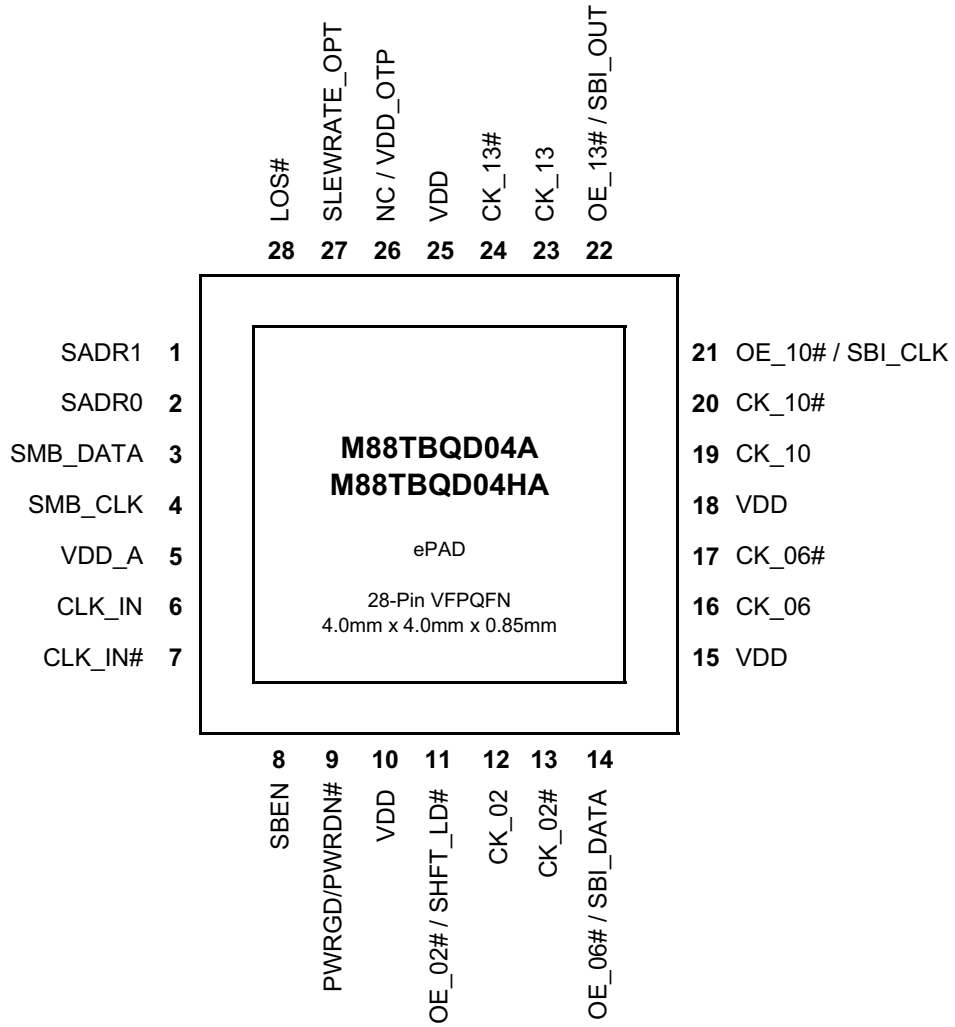
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Figure 5. M88TBQD08 Pin Assignment



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Figure 6. M88TBQD04 Pin Assignment



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Figure 7. M88TBSQ2KL Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	
A	CK_17	CK_16#	CK_16	CK_15#	CK_15	CK_14#	CK_14	CK_13#	CK_13	CK_12#	CK_12	CK_11#	A
B	CK_17#	VDD	NC/ OE_16#	SADR0	NC/ OE_15#	VDD	NC/ OE_14#	SADR1	NC/ OE_13#	OE_12#	VDD	CK_11	B
C	CK_18	NC/ SBI_OUT									OE_11#	CK_10#	C
D	CK_18#	NC/ OE_17#									NC/ OE_18#	CK_10	D
E	CK_19	SBEN									OE_10#/ SHFT_LD#	OE_09#	E
F	CK_19#	NC/CLK_ IN_IR									NC/ PRST#	CK_09#	F
G	CLK_IN	NC/CLK_ IN_IR#									NC/ LOS#	CK_09	G
H	CLK_IN#	VDD_A									OE_08#	CK_08#	H
J	CK_00	NC/ OE_00#									NC/ OE_19#	CK_08	J
K	CK_00#	NC/ OE_01#									OE_07#	CK_07#	K
L	CK_01	VDD	NC/ OE_02#	SMB_DA TA	SMB_CL K	NC/ OE_03#	NC	OE_05#/ SBI_DAT A	NC/ OE_04#	OE_06#/ SBI_CLK	VDD	CK_07	L
M	CK_01#	CK_02	CK_02#	CK_03	CK_03#	PWRGD/ PWRDN#	CK_04	CK_04#	CK_05	CK_05#	CK_06	CK_06#	M
	1	2	3	4	5	6	7	8	9	10	11	12	

M88TBSQ2KLA
M88TBSQ2KLHA

ePAD

80-Pin GQFN
6.0mm x 6.0mm x 0.75mm

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Figure 8. M88TBSQD12 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	
A	LOS#	CK_00#	CK_00	CK_01#	CK_01	CK_02#	CK_02	CK_03#	CK_03	OE_04# /SBI_CLK	A
B	SADR1	NC	OE_00#	OE_01#	VDD	NC	OE_02# /SBI_OUT	OE_03#	NC	CK_04#	B
C	SADR0	SLEWRATE _OPT							VDD	CK_04	C
D	SMB_CLK	SMB_DATA		GND	GND	GND	GND		NC	CK_05#	D
E	CLK_IN	NC/CLK_IN _IR		GND	GND	GND	GND		OE_05#	CK_05	E
F	CLK_IN#	VDD_A		GND	GND	GND	GND		NC/PRST#	CK_06#	F
G	OE_11#	NC/CLK_IN _IR#		GND	GND	GND	GND		OE_06#	CK_06	G
H	CK_11	VDD							VDD	CK_07#	H
J	CK_11#	NC	VDD	OE_10# /SHFT_LD#	NC	OE_09#	NC	OE_08#	NC	CK_07	J
K	SBEN	PWRGD /PWRDN#	NC	CK_10	CK_10#	CK_09	CK_09#	CK_08	CK_08#	OE_07# /SBI_DATA	K
	1	2	3	4	5	6	7	8	9	10	

M88TBSQD12A
M88TBSQD12HA

64-Pin LGA
5.0mm x 5.0mm x 0.66mm

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Ordering Information

Part Number	Package	Number of Outputs	Differential Output Impedance (Ω)	Carrier Type	Temperature (°C)
M88TBQ2KA-T	72-pin QFN, 10.0mm x 10.0mm x 0.9mm	20	85	Tape & Reel	−40 to +105
M88TBQ2KHA-T			100		
M88TBQ2KLA-T	80-pin GQFN, 6.0mm x 6.0mm x 0.75mm	20	85	Tape & Reel	−40 to +105
M88TBQ2KLHA-T			100		
M88TBQD16A-T	64-pin VFPQFN, 9.0mm x 9.0mm x 0.75mm	16	85	Tape & Reel	−40 to +105
M88TBQD16HA-T			100		
M88TBQD12A-T	64-pin LGA, 5.0mm x 5.0mm x 0.66mm	12	85	Tape & Reel	−40 to +105
M88TBQD12HA-T			100		
M88TBQD08A-T	40-pin VFPQFN, 5.0mm x 5.0mm x 0.75mm	8	85	Tape & Reel	−40 to +105
M88TBQD08HA-T			100		
M88TBQD04A-T	28-pin VFPQFN, 4.0mm x 4.0mm x 0.85mm	4	85	Tape & Reel	−40 to +105
M88TBQD04HA-T			100		
M88TBSQ2KLA-T	80-pin GQFN, 6.0mm x 6.0mm x 0.75mm	20	85	Tape & Reel	−40 to +105
M88TBSQ2KLHA-T			100		
M88TBSQD12A-T	64-pin LGA, 5.0mm x 5.0mm x 0.66mm	12	85	Tape & Reel	−40 to +105
M88TBSQD12HA-T			100		

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