

Description

M88DR5RCD02 is a two-channel, single-ended DDR5 Registering Clock Driver (RCD) with parity for driving and buffering the Command/Address (CA) bus, Chip Selects, and clock between the host controller and the DDR5 SDRAMs. It also creates a BCOM bus used to control the Data Buffers (DBs) for LRDIMMs.

The two separate channels have some common logic but operate independently. Each has a DDR/SDR CA bus input, a single parity input, two Chip Select (CS) inputs, and produces two copies of SDR CA bus outputs and two copies of CS outputs.

M88DR5RCD02 supports DDR and SDR on the Host Command/Address signals, with a maximum speed up to 5600 MT/s. The Chip Select is SDR for both settings on DCA and QCA. Commands are sent to a single rank or multiple ranks, and the ODT control is encoded into Chip Selects.

M88DR5RCD02 supports register access mechanisms through a sideband bus or in-band channel commands. Control Word registers (CW) are configurable to optimize the RCD properties for different DIMM raw card designs.

Features

- Fully compliant with JEDEC DDR5RCD02 specification

- Speed up to 5600 MT/s
- 1.1V V_{DD} and 1.0V V_{DDIO} Voltage
- Two-channel 1:2 registering buffer for DDR or SDR Command/Address inputs and control signals
- Integrated PLL clock driver distributing one differential clock input to five differential clock pairs per channel
- Dual chip selects
- Parity checking across CA and DPAR inputs separately on two sub-channels
- Output characteristics configurable through Register Words
- CS, CA and DFE calibration training modes
- Dual Frequency support
- ZQ calibration
- Latency equalization
- Output delay control
- Sideband bus interface
 - I²C FM+ mode (1MHz)
 - I³C basic mode (up to 12.5 MHz)
- Power saving modes
 - PDE power down mode
 - PDE power down mode with ODT control
 - Self Refresh mode with/without Clock Stop
- Green package: 240-ball FCBGA
- RoHS compliant

Applications

- High-performance DDR5 RDIMMs

RDIMM Application Example

