

Description

The M88P5010 / M88P5000 is a JEDEC-compliant Power Management IC (PMIC) for DDR5 server DIMM applications. It contains 4 DC-DC buck converters and low-dropout regulators (LDO, 1.8 V and 1.0 V).

The PMIC is designed to provide power support for other on-DIMM chips such as DRAM, RCD, DB, SPD Hub, and TS. The CPU implements power management by communicating with the PMIC via the SPD Hub.

M88P5010 is designed for low-current RDIMMs, and M88P5000 for high-current RDIMMs and LRDIMMs.

Features

- Compliant with JEDEC DDR5 server low/high current PMIC5010/PMIC5000 DIMM application
 - M88P5010
 - * 4 buck converters (SWA, SWB, SWC and SWD) with per phase current capability of 3A full load / 3.5A peak load, and two LDOs of VLDO_1.8V and VLDO_1.0V
 - * SWA and SWB can be also configured into one-output converter with dual-phase to provide 6A full load/ 7A peak load
 - M88P5000
 - * 4 buck converters (SWA, SWB, SWC and SWD) with per phase current capability of

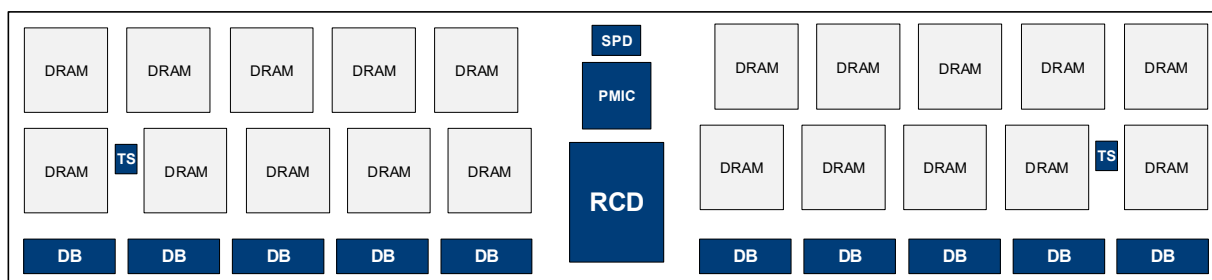
5A full load / 6A peak load, and two LDOs of VLDO_1.8V and VLDO_1.0V

- * SWA and SWB can be also configured into one-output converter with dual-phase to provide 10A full load/ 12A peak load
- Wide VIN_BULK voltage range to support 12V power supply in normal case and 5V power supply mainly in Switch-Over case
- COT structure to provide fast transient load response
- Selectable FCCM or DCM operation
- Configurable Power On and Power Off sequence with programmable Soft-Start / Soft-Stop time
- Voltage, output current, output power and temperature reporting
- Input supply Switch Over function to provide uninterrupted operation
- I²C and I³C Basic interfaces
- Non-Write Protect mode for debug and validation
- Protection functions, such as OVP, UVP, OCL and OTP with error log counter and data storage
- 5x5 35-pin FCQFN package

Applications

- DDR5 Server DIMM
 - M88P5010: Low-current RDIMM
 - M88P5000: High-current RDIMM and LRDIMM

Application Example (for LRDIMM)



Application Example (for RDIMM)

