Description

The M88DR5CK01 is Montage's 1st-generation DDR5 Clock Driver (CKD) chip for use in the client memory to buffer the clock between the Host controller and DRAMs, and enhance the speed and stability of memory data access.

The M88DR5CK01 has three clock driving modes: Single PLL Mode, Dual PLL mode and PLL Bypass Mode (Legacy mode). In Single PLL mode, the device uses one input clock pair to produce four separate output clock pairs to the two DRAM channels. In Dual PLL mode, the device uses two input clock pairs to produce four separate output clock pairs to the two DRAM channels. In PLL Bypass mode, the device uses four input clock pairs to produce four separate output clock pairs to the two DRAM channels.

By configuring the control register settings, the device can change its output characteristics to match different DIMM net topologies. By disabling unused outputs, the power consumption is reduced.

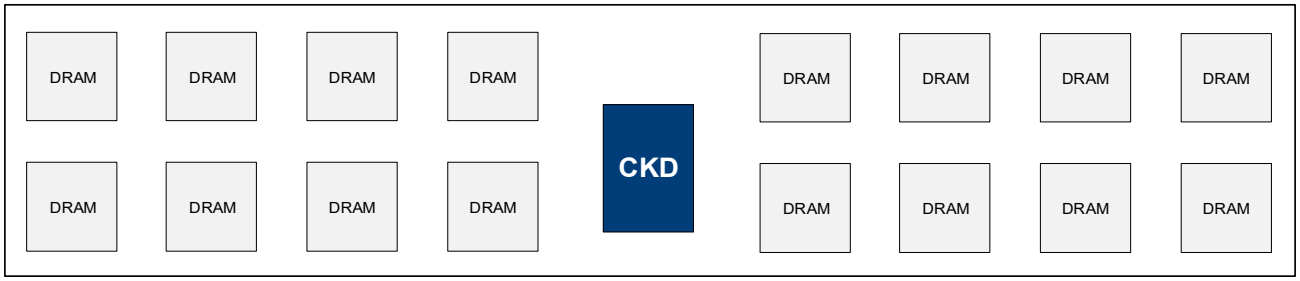
Features

- Compliant with JEDEC Clock Driver Definition (DDR5CKD01) specification
- Speed up to DDR5-7200
- 1.1V VDD voltage support
- Output characteristics configurable through control registers
- Clock driver with zero phase delay
- Programmable latency per channel
- I^2C and I3C Basic interface
- Dual-sideband Bus address
- Ultra-low power consumption
- RoHS compliant
- Green package: 35-ball Fine-Pitch Ball Grid Array (FPBGA)

Applications

- DDR5 CUDIMM, CSODIMM and CAMM

Application Example (for CUDIMM or CSODIMM)



For more information on the product, please contact globalsales@montage-tech.com