

## Description

M88MR5DB01 is a dual 4-bit bidirectional Multiplexed Data Buffer (MDB) with differential strobes designed for 1.1 V  $V_{DD}$  operation. With a dual-nibble host bus interface connected to a memory controller, it supports x4 mode and x8 mode on the DRAM interface and is configurable to two nibbles for x4 DRAMs or one byte for x8 DRAMs. It also has an input-only control bus interface connected to the DDR5MRCD01, and this interface consists of a 3-bit control bus, a reset signal, a Chip Select input and a differential clock input.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are  $V_{DD}$  terminated drivers optimized to drive single or dual terminated traces in MRDIMM / MCRDIMM applications. Differential DQS signals are used to sample the DQ inputs and are regenerated internally.

M88MR5DB01 supports dedicated pins for ZQ calibration.

The device features a set of 8-bit control words, which can be configured to improve the device properties for different raw card designs.

## Features

- Compliant with Intel DDR5 MCR Spec. Rev 0.99
- Speed up to 8800 MT/s
- Dual 4-bit bidirectional data register
- x4/x8 DRAMs supported
- Up to 2 package ranks per pseudo-channel

- Separate transfers handled on 2 pseudo-channels
- Regeneration of DQS signals from input clock
- Early swizzle discovery prior to QCS training
- FIFOs on DQ path for decoupling Host and DRAM interface time domains
- Independent internal Vref control for Host, DRAM and BCOM interfaces
- ZQ calibration
- BCOM Training Mode
- Per X addressability modes:
  - Per DRAM Addressability (PDA) mode
  - Per Buffer Addressability (PBA) mode
  - PBA Enumerate ID programming
  - PBA Select ID operation
- Strobe and Data Training
- DRAM Periodic Update
- DQ Pass-through Mode
- Transparent Mode, Continuous Burst Mode, and Loopback Mode for debugging/testing/training
- CTLE and 6-tap DFE integrated on host-interface receivers
- Power-saving modes:
  - PDE Power Down
  - Self Refresh with/without Clock Stop
- 1.1V  $V_{DD}$  with ultra-low power consumption
- Green package: 78-ball FBGA
- RoHS compliant

## Applications

- DDR5 MRDIMM / MCRDIMM

### MRDIMM / MCRDIMM Application Example

