

Description

M88TB(S)2205M^{1,2,3,4} is a series of high-performance clock fanout buffers with 5 outputs. The buffer is designed for low-jitter, high-frequency clock/data distribution and level translation applications.

The buffer supports clock input selection from either one differential clock pair or one crystal input, distributing the selected clock to two output banks, which consist of 2 differential clock pairs and 3 single-ended LVCMOS output clocks, respectively.

Operating with a core supply of 1.8V-3.3V and supplies of 1.8V-3.3V for differential outputs and 1.5V-3.3V for single-ended outputs, the M series clock buffer provides flexible control via logic pins for input reference clock selection, differential I/O type selection, and output enable/disable functions.

The buffer can be paired with Montage Technology's M88TG010xx clock generator to deliver a robust clock tree solution. With broad input and output frequency ranges, optimized power management, and reduced propagation delay, the buffer operates across a wide temperature range, making it an ideal choice for demanding applications.

Features

- 2 input clocks:
 - 1 differential clock pair supporting up to 3.1GHz, and accepting single-ended clock source up to 350MHz
 - 1 crystal input, accepting 8MHz to 50MHz crystal or single-ended clock source
- 5 output clocks:
 - 2 output banks, containing 2 differential clock pairs in Bank A and 3 LVCMOS output clocks in Bank B

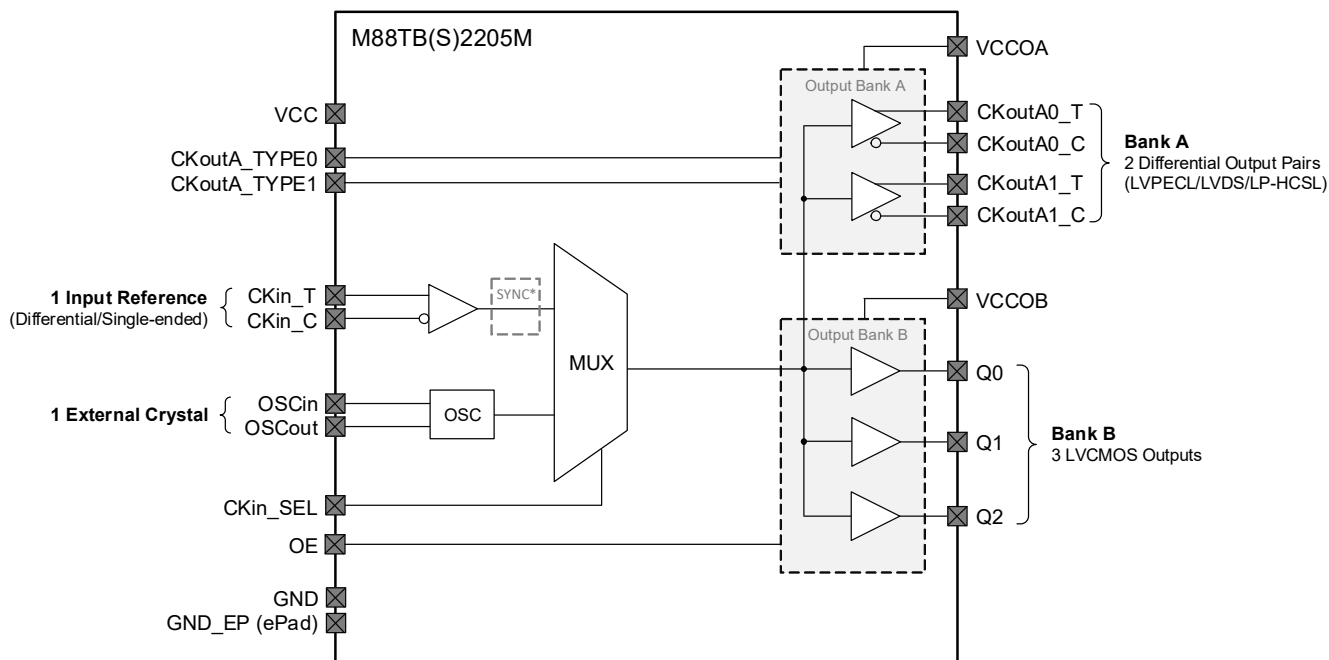
1. TBS: Includes glitch-free switchover.
2. TB: No glitch-free switchover.
3. M: Supports an output pattern of both differential clock pairs and single-ended clocks.
4. Unless otherwise stated, the terms "M series clock buffer", "clock buffer" and "buffer" refer to the entire series.

- Frequency range:
 - LVCMOS: DC to 350MHz
 - LVDS: DC to 3.1GHz
 - LVPECL: DC to 3.1GHz
 - LP-HCSL: DC to 1GHz
- Excellent PSRR:
 - LVDS: -74dBc @ 156.25MHz
 - LVPECL: -67dBc @ 156.25MHz
 - LP-HCSL: -76dBc @ 156.25MHz
- Ultra-low latency and skew
- Additive jitter:
 - 34 fs RMS (12kHz to 20MHz) typical @ LP-HCSL 156.25MHz
 - 10 fs RMS typical @ PCIe[®] Gen 5 jitter (CC)
- Configurable power supplies:
 - Differential outputs: 1.8V-3.3V
 - Single-ended outputs: 1.5V-3.3V
 - Core: 1.8V-3.3V
- Pin-based control for flexible input reference clock selection, output I/O type selection and output enable/disable
- Glitch-free switchover supported in M88TBS2205M
- Working temperature: -40°C to +85°C
- Package: 24-pin WQFN

Applications

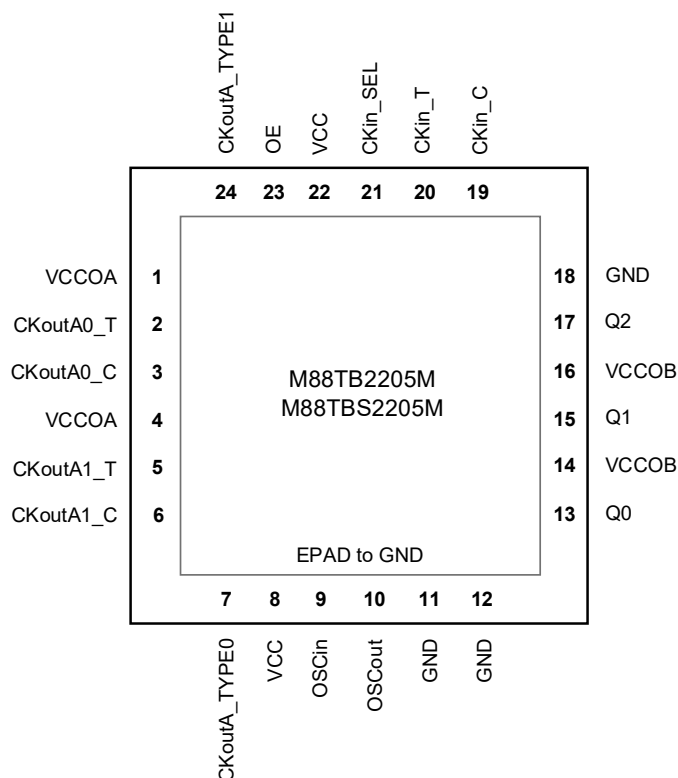
- Clock distribution and level translation for ADCs, DACs, SATA/SAS, SONET/SDH, multi-gigabit Ethernet, and Fibre Channel line cards
- Servers, storage systems, switches, routers, and display panels
- PCIe Gen 1 to Gen 6 and NVLink
- Reference clock distribution for BBU and RRU applications

Functional Block Diagram



Note: Only the TBS version (includes glitch-free switchover) supports the synchronization function.

Pin Assignment (24-Pin WQFN, 4.0mm x 4.0mm x 0.75mm)



Ordering Information

Part Number	Package	Operating Temperature
M88TB2205M	24-pin WQFN, 4.0mm x 4.0mm x 0.75mm	-40°C to +85°C
M88TBS2205M		