Description

M88TB(S)2310A[1,2,3,4] is a type of high-performance clock fanout buffers operating at up to 3.1GHz with 10 outputs. The buffer is designed for low-jitter, high-frequency clock/data distribution and level translation.

The buffer supports clock input selection from either two differential clock pairs or a crystal input, distributing the selected clock to two output banks, each with 5 differential outputs, along with a dedicated LVCMOS output. Both differential output banks can be configured as LVPECL, LVDS, LP-HCSL, or disabled.

Operating with a core supply of 1.8V-3.3V and three independent output supplies of 1.8V-3.3V, the clock buffer provides flexible control via logic pins for input reference clock selection, differential output type selection and output enable/disable functions.

The buffer can be paired with Montage Technology's M88TG010xx clock generator to deliver a robust clock tree solution. With broad input and output frequency ranges, optimized power management, and reduced propagation delay, the buffer operates across a wide temperature range, making it an ideal choice for demanding applications.

Features

- 3 input reference clocks:
  - 2 differential clock pairs up to 3.1GHz, accepting single-ended clock source up to 350MHz
  - 1 crystal input, accepting 8MHz to 50MHz crystal or single-ended clock source
- 10 output clocks:
  - 2 power banks with 5 differential outputs each, supporting LVPECL, LVDS and LP-HCSL
  - 1 independent LVCMOS output clock
- Frequency range:
  - LVCMOS: DC to 350MHz
  - LVDS: DC to 3.1GHz
  - LVPECL: DC to 3.1GHz
  - LP-HCSL: DC to 1GHz
- Additive jitter:
  - 34 fs RMS (12kHz to 20MHz) typical @ LP-HCSL 156.25MHz
  - 10 fs RMS typical @ PCIe® Gen 5 jitter (CC)
- Excellent PSRR:
  - LVDS: -74dBc @ 156.25MHz
  - LVPECL: -67dBc @ 156.25MHz
  - LP-HCSL: -76dBc @ 156.25MHz
- Ultra-low latency and skew
- Three independently configurable 1.8V-3.3V power supplies for:
  - Core
  - Differential outputs
  - Single-ended outputs
- Pin-based control for flexible input reference clock selection, output type selection and enable/disable
- Glitch-free switchover supported in TBS version
- Working temperature: -40°C to +85°C
- Package: 48-pin WQFN

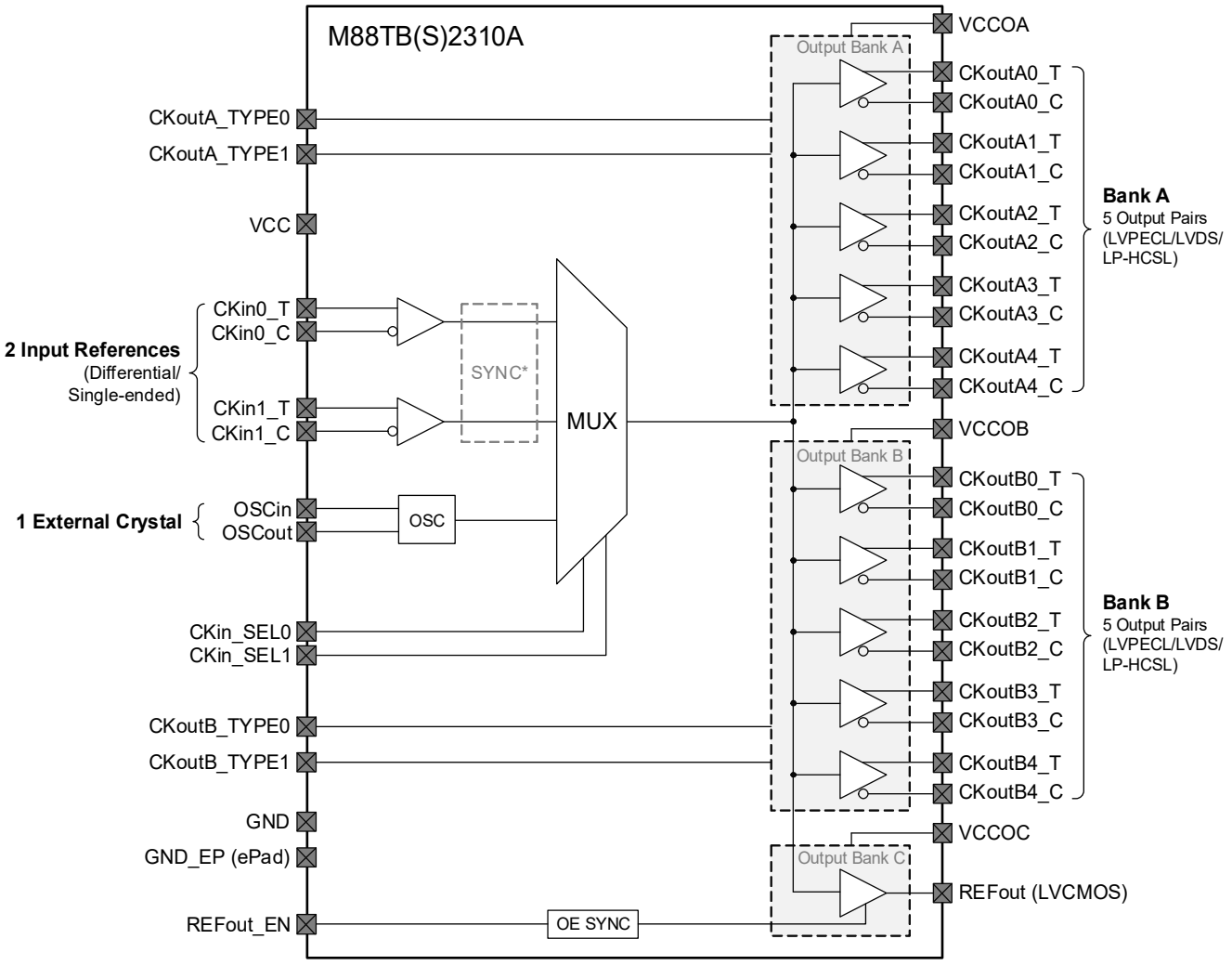
Applications

- Clock distribution and level translation for ADCs, DACs, SATA/SAS, SONET/SDH, multi-gigabit Ethernet, and Fibre Channel line cards
- Servers, storage systems, switches, routers, and display panels
- PCIe Gen 1 to Gen 6 and NVLink
- Reference clock distribution for BBU and RRU applications

1. TB: No glitch-free switchover.
2. TBS: Includes glitch-free switchover.
3. A: Supports LVPECL, LVDS, and LP-HCSL differential clock outputs.
4. Unless otherwise stated, the terms "clock buffer" and "buffer" refer to the entire series.

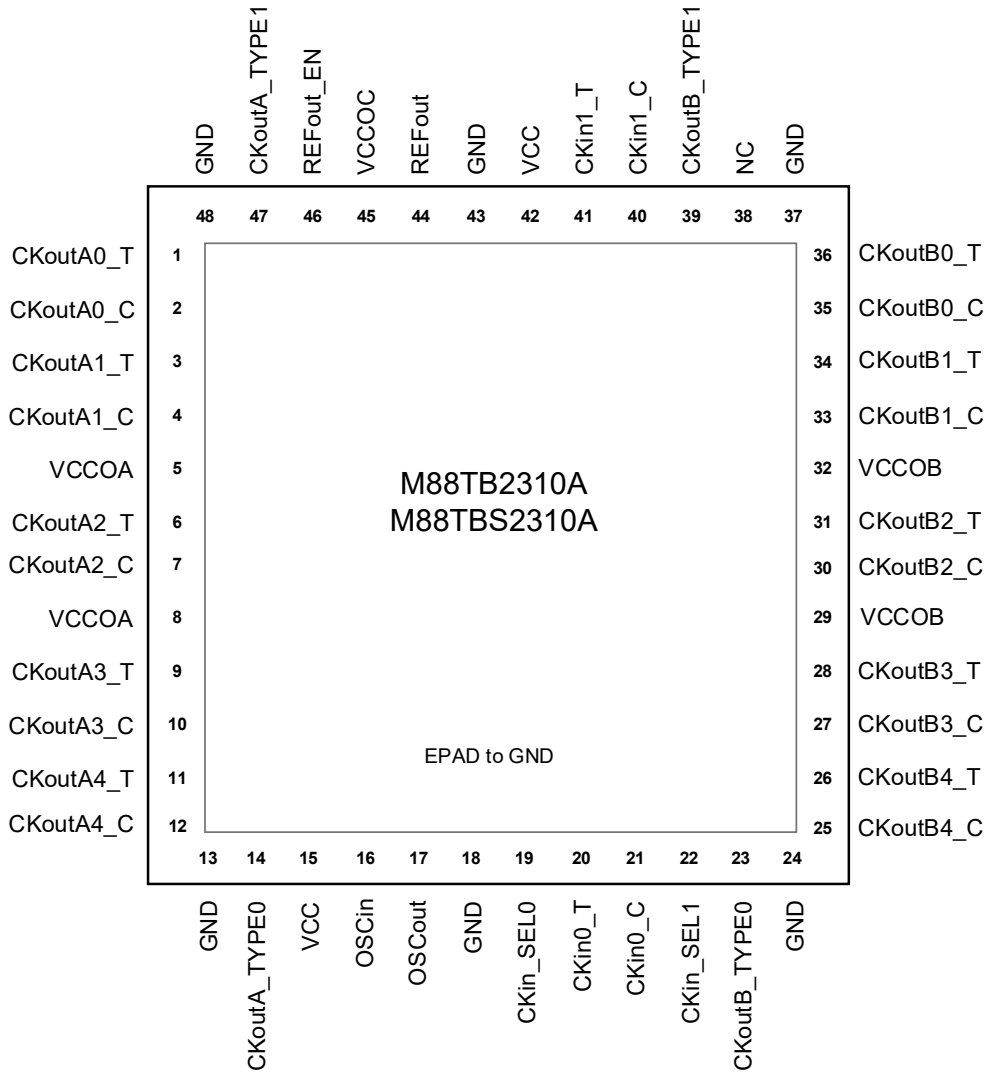
For more information on the product, please contact globalsales@montage-tech.com

Functional Block Diagram



Note: Only the TBS version (includes glitch-free switchover) supports the synchronization function.

Pin Assignment (48-pin WQFN, 7.0mm x 7.0mm x 0.75mm)



Ordering Information

Part Number	Package	Operating Temperature
M88TB2310A	48-pin WQFN, 7.0mm x 7.0mm x 0.75mm	-40°C to +85°C
M88TBS2310A		