

Description

M88TB(S)1310C^{1,2,3} is a type of high-performance clock fanout buffers operating at up to 350MHz with 10 single-ended outputs. The buffer is designed for low-jitter, high-frequency clock/data distribution and level translation applications.

The buffer supports clock input selection from either two differential clock pairs or one crystal input, distributing the selected clock to one output bank.

Operating with a core supply of 1.8V-3.3V and output supplies of 1.5V-3.3V, the clock buffer provides flexible control via logic pins for input reference clock selection and output enable/disable functions.

The buffer can be paired with Montage Technology's M88TG010xx clock generator to deliver a robust clock tree solution. With broad input and output frequency ranges, optimized power management, and reduced propagation delay, the buffer operates across a wide temperature range, making it an ideal choice for demanding applications.

Features

- 3 input reference clocks:
 - 2 differential clock pairs, supporting up to 350MHz for both differential and single-ended clock sources
 - 1 crystal input, accepting 8MHz to 50MHz crystal or single-ended clock source
- 10 output clocks:
 - 10 independent LVCMOS output clocks in one bank

1. TBS: Includes glitch-free switchover.

2. TB: No glitch-free switchover.

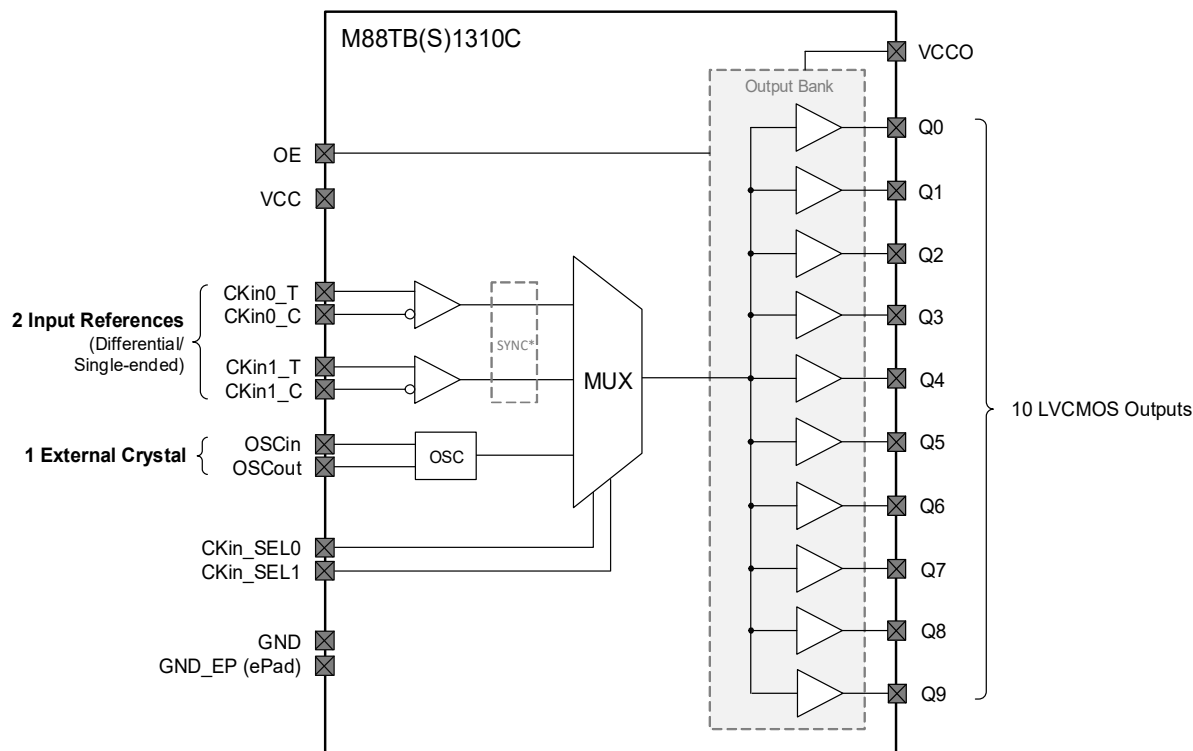
3. Unless otherwise stated, the terms "clock buffer" and "buffer" refer to the entire series.

- Frequency range: DC to 350MHz
- Excellent PSRR: -53dBc (LVCMOS) @ 156.25MHz
- Ultra-low latency and skew
- Additive jitter:
 - 34 fs RMS (12kHz to 20MHz) typical @ LVCMOS 156.25MHz
- Configurable power supplies:
 - Core: 1.8V-3.3V
 - Single-ended outputs: 1.5V-3.3V
- Pin-based control for flexible input reference clock selection and output enable/disable
- Glitch-free switchover supported in TBS version
- Working temperature: -40°C to +85°C
- Package: 32-pin WQFN

Applications

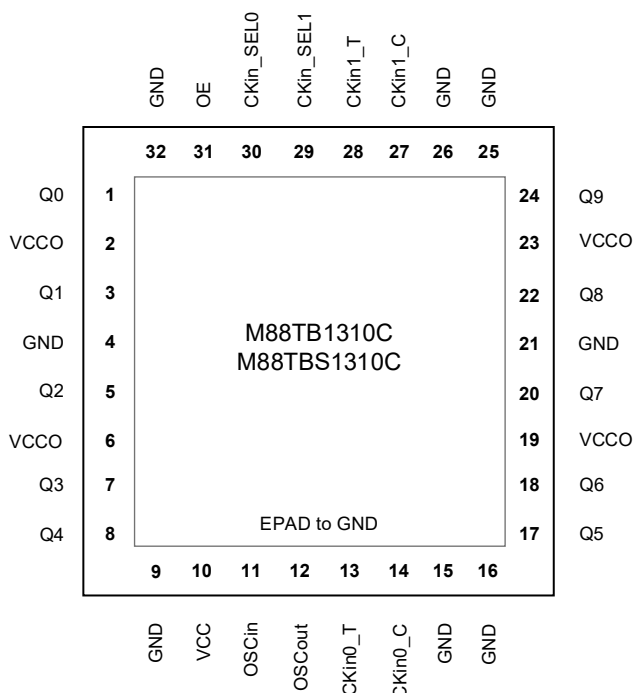
- Clock distribution and level translation for ADCs, DACs, SATA/SAS, SONET/SDH, multi-gigabit Ethernet, and Fibre Channel line cards
- Servers, storage systems, switches, routers, and display panels
- PCIe® Gen 1 to Gen 6 and NVLink
- Reference clock distribution for BBU and RRU applications

Functional Block Diagram



Note: Only the TBS (includes glitch-free switchover) version supports the synchronization function.

Pin Assignment (32-Pin WQFN, 5.0mm x 5.0mm x 0.75mm)



Ordering Information

Part Number	Package	Operating Temperature
M88TB1310C	32-pin WQFN, 5.0mm x 5.0mm x 0.75mm	-40°C to +85°C
M88TBS1310C		