

Description

M88TG0102A/B is a Clock Generator with one input reference clock, two programmable output pairs plus one LVCMOS reference output.

The chip utilizes Montage's advanced IO technology to generate a wide range of frequencies with excellent jitter performance for low phase noise spread-spectrum applications such as PCIe. It can source multiple 100MHz PCIe clock outputs. All differential clock outputs are compliant to PCIe Gen1/2/3/4/5/6 common clock and separate reference clock architecture specifications.

This chip supports the initialization through on-chip One-Time Programmable (OTP) configuration. These chip configurations can be partly or fully modified in working state according to the current control mode decided by a strapping pin at power-up stage, which easily realizes software selection of the desired configuration. Four programmable I²C addresses are available, allowing easy I²C access to multiple components.

Features

General

- 2-output programmable clock generator
- High jitter performance
- Working temperature: -40°C ~ 85°C
- Power supply: 1.8V to 3.3V
- Low power consumption
 - < 100mW (1.8V with 100MHz LP-HCSL outputs)
- Input reference source option
 - M88TG0102A: external crystal or clock input
 - M88TG0102B: internal crystal

Input Reference Clock

- Single input source
 - Crystal input source
 - * Internal crystal: 50MHz, or
 - * External crystal: 8MHz ~ 50MHz
 - Clock input source
 - * Frequency range: 1.22MHz ~ 250MHz
 - * Acceptable input duty cycle: 40 ~ 60%

Output Clock

- 2 differential-pair outputs

- Output frequency range: 1MHz ~ 333.33MHz
- Montage-developed LP-HCSL for high jitter performance and low power
- Support LVPECL and CML logic with easy AC coupling
- 1 LVCMOS reference clock output
- Support all three PCIe clocking architectures
 - Common Clocked (CC)
 - Independent Reference without spread spectrum (SRnS)
 - Independent Reference with spread spectrum (SRIS)
- Optional individual SSC setting for all output clocks; feedback fractional divider used by SSC for better jitter performance
- Programmable output impedance: 85Ω, 100Ω or off

Control

- Three control modes selectable at power-on stage: I²C mode, OTP mode, PIN mode
- Output clock dynamical control by multi-function pins
- Support up to 4 On-chip OTP configurations
- Four programmable I²C addresses: D0, D2, D4, D6

Package

- 3.0mm x 3.0mm x 1.1mm, 0.5mm pitch 16-pin LGA
- Package MSL: Level-2-260C

Key Specifications

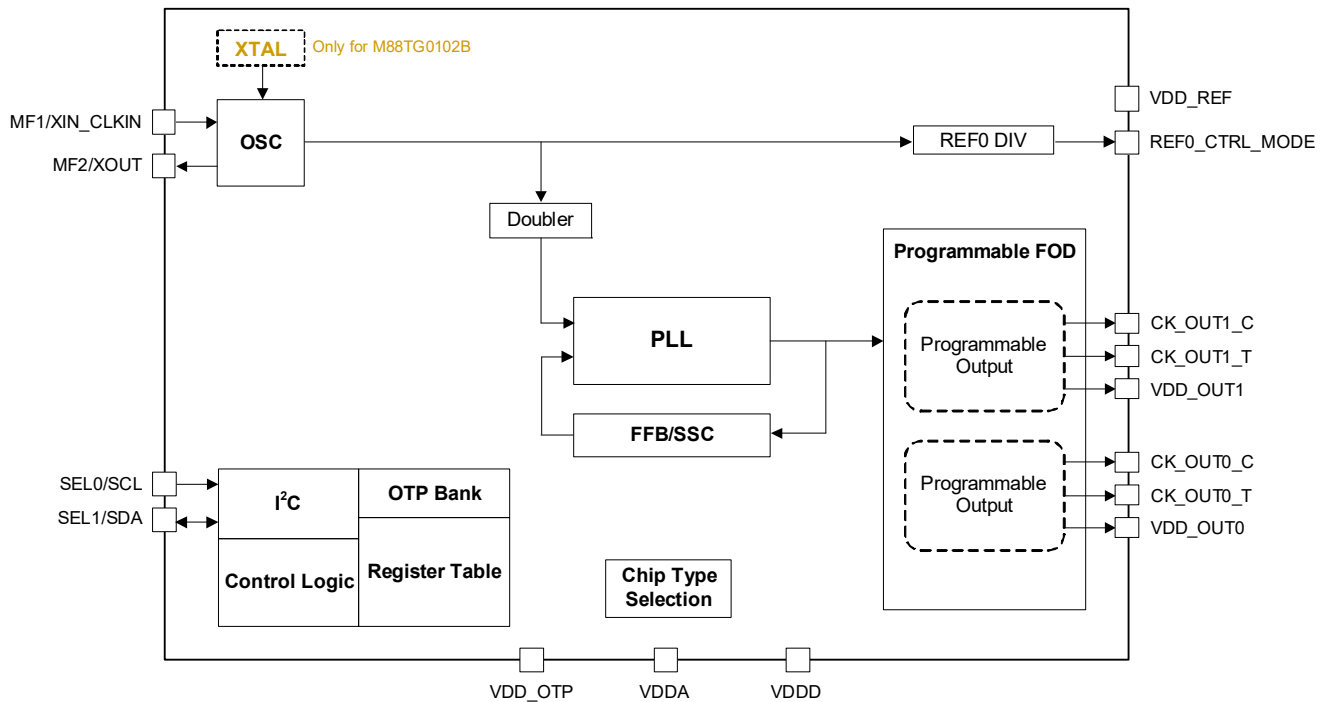
- 250fs RMS 12kHz-20MHz typical phase jitter at 100MHz
- 230fs RMS 12kHz-20MHz typical phase jitter at 156.25MHz
- FFB PCIe Gen5 jitter (CC) typical 30fs RMS
- FOD PCIe Gen5 jitter (CC) typical 98fs RMS
- FFB PCIe Gen6 jitter (CC) typical 20fs RMS
- FOD PCIe Gen6 jitter (CC) typical 66fs RMS

Applications

- High-performance Computing (HPC)
- Storage, like SSD
- Ethernet
- Fiber Optic Modules
- NVLink

Functional Block Diagram

Figure 1. M88TG0102A/B Block Diagram

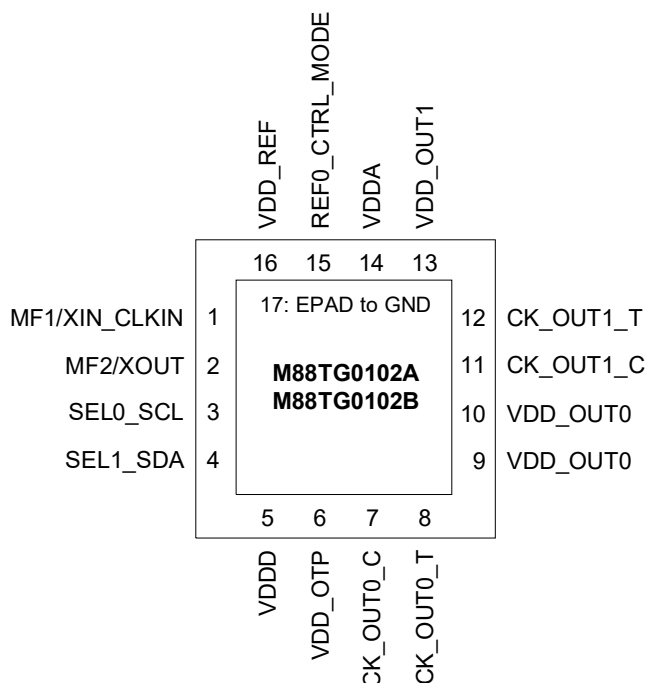


Notes:

1. FFB: Fraction Feedback Divider
FOD: Fraction Output Divider
IN DIV: Input Divider
OTP: One-Time Programmable
PLL: Phase Locked Loop
SSC: Spread Spectrum Clocking
XTAL: Crystal

1 Pin Diagram

Figure 2. 16-LGA Pin Assignment, 3.0mm x 3.0mm x 1.1mm, 0.5mm Pitch (Top view)



2 Ordering Information

Part Number	Package	Temperature	Crystal	Packing
M88TG0102A-XX	3mm x 3mm x 1.1mm, 0.5mm pitch 16-LGA; MSL Level-2-260C	-40 ~ +85°C	External	Tray
M88TG0102A-XX-T				Tape & Reel
M88TG0102B-XX	3mm x 3mm x 1.1mm, 0.5mm pitch 16-LGA; MSL Level-2-260C	-40 ~ +85°C	50MHz Internal	Tray
M88TG0102B-XX-T				Tape & Reel