

Description

M88DR4RCD02P is a 32-bit 1:2 configurable registering clock driver with parity for driving address and control nets on DDR4 RDIMM, LRDIMM and NVDIMM applications.

The device accepts 32 bits address and control signals and outputs two copies per signal. It includes a parity checking function, which compares an input parity bit with the corresponding data input.

The command, address and control bus inputs are pseudo-differential with an external or internal voltage reference. The outputs of these signals are full swing CMOS drivers optimized to drive single terminated 25 Ω to 50 Ω traces in various DIMM applications.

M88DR4RCD02P has three basic modes of operation associated with the DA[1:0] bits in the DIMM configuration control word (F0RC0D).

The device operates from the differential clock pair (CK_t and CK_c). The input signals could be either re-driven to the outputs, or used to access device internal control registers when certain conditions are met.

Control register settings are configurable to change output characteristics for different DIMM topologies.

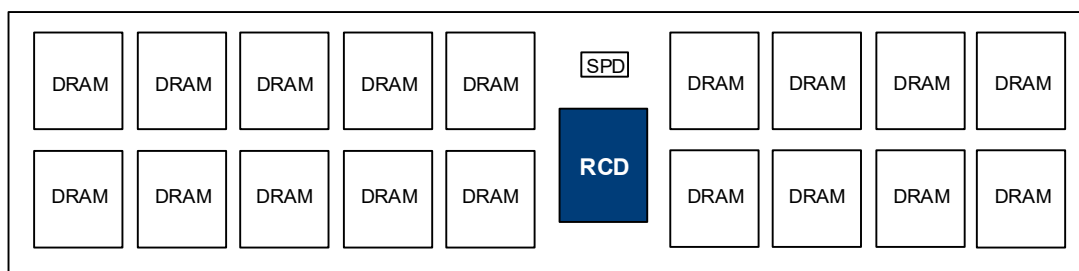
Features

- Fully compliant with JEDEC DDR4RCD02 specification
- Speed up to DDR4-3200
- 32-bit 1:2 registering buffer for address and control signals
- Integrated PLL clock driver distributing one differential clock pair to five differential pairs
- 1.2V V_{DD} Voltage
- Dual and Quad chip selects
- Parity checking on command and address inputs
- Constant propagation delay with VT variations
- ZQ calibration of Ron and IBT values
- Programmable latency equalization
- CA bus training mode support to align the incoming CA and CTRL signals optimally
- I²C Bus interface
- Different power saving modes such as S3 low power mode and CK stop mode
- Ultra-low power consumption
- Green package: 253-ball FBGA
- RoHS compliant

Applications

High-performance DDR4 RDIMMs, LRDIMMs and NVDIMMs

RDIMM Application Example



LRDIMM Application Example

