Description

M88DDR4DB01 is a dual 4-bit bidirectional data buffer with differential strobes. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 register buffer. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

All data (DQ) inputs are pseudo-differential with an internal voltage reference. All DQ outputs are V_{DD} terminated drivers optimized to drive single or dual terminated traces in DDR4 LRDIMM applications. The differential data strobe (DQS) signals are used to sample the DQ inputs and are regenerated internally for driving out the DQ outputs on the opposite side of the device.

The control inputs BCOM[3:0], BCKE and BODT are sampled by the clock inputs BCK_t and BCK_c. M88DDR4DB01 also supports dedicated pins for ZQ calibration and for parity and sequence error alerts.

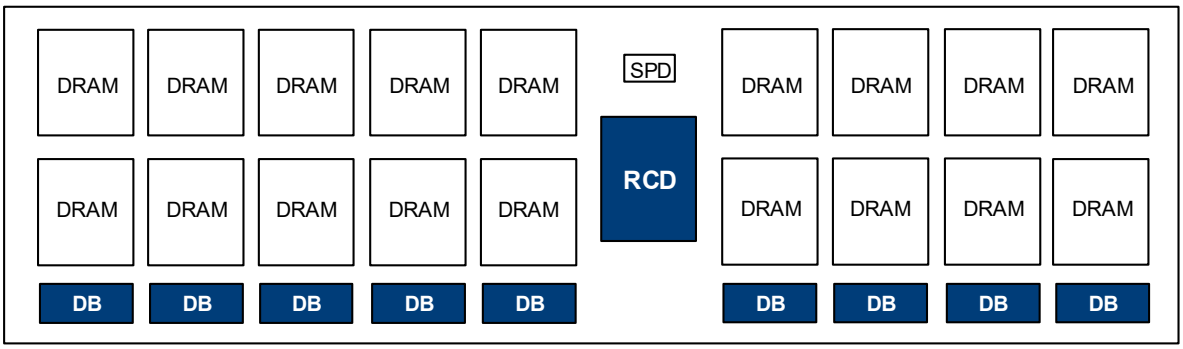
Features

- Fully compliant with JEDEC DDR4DB01 specification
- Support up to DDR4-2400
- Bidirectional retiming and 1:1 redriving of DDR4 DQ signals
- Regeneration of DQS signals from input clock
- FIFOs on the DQ path for decoupling Host and DRAM interface time domains
- Up to four package ranks supported
- Package rank timing alignment supported on the Host interface
- Only x4 DRAM devices supported
- Internally generated VrefDQ and independent control on Host interface and DRAM interface
- 1.2V V_{DD} Voltage
- Parity error checking and sequence error checking on the BCOM interface
- DQ/MDQ input and output characteristics configurable through control registers
- Constant propagation delay from input clock to output DQ/MDQ with VT variations
- ZQ calibration of Ron and IBT values
- Synchronous ODT mode supported including a RTT_PARK feature (in addition to RTT_NOM and RTT_WR)
- Various DQ calibration support features
- Per DRAM Addressability (PDA) feature
- Per Buffer Addressability (PBA) feature
- Programmable write and read preamble
- Read Preamble training feature
- BCW read mode and MPR read override mode supported
- Input clock frequency change and dual frequency context switching supported
- Different power saving modes such as CKE low power mode and CK stop mode
- Ultra-low power consumption
- Memory BIST and transparent mode supported
- Green package: 53-ball FBGA
- RoHS compliant

Applications

- High-performance DDR4 LRDIMMs

LRDIMM Application Example



For more information on the product, please contact globalsales@montage-tech.com